



FIG. 1

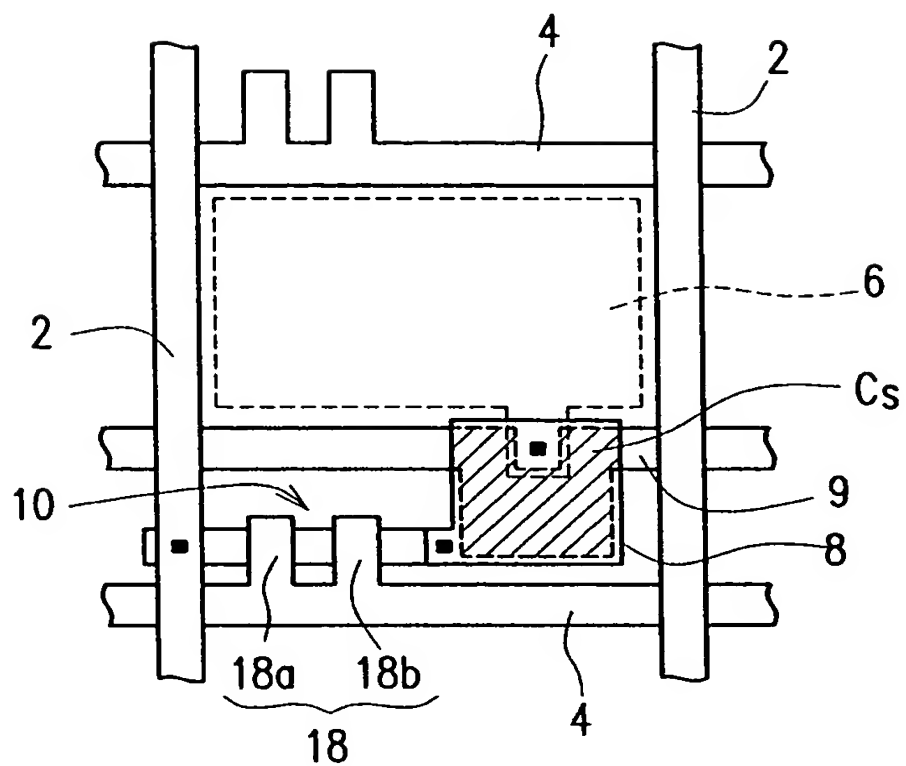


FIG. 2

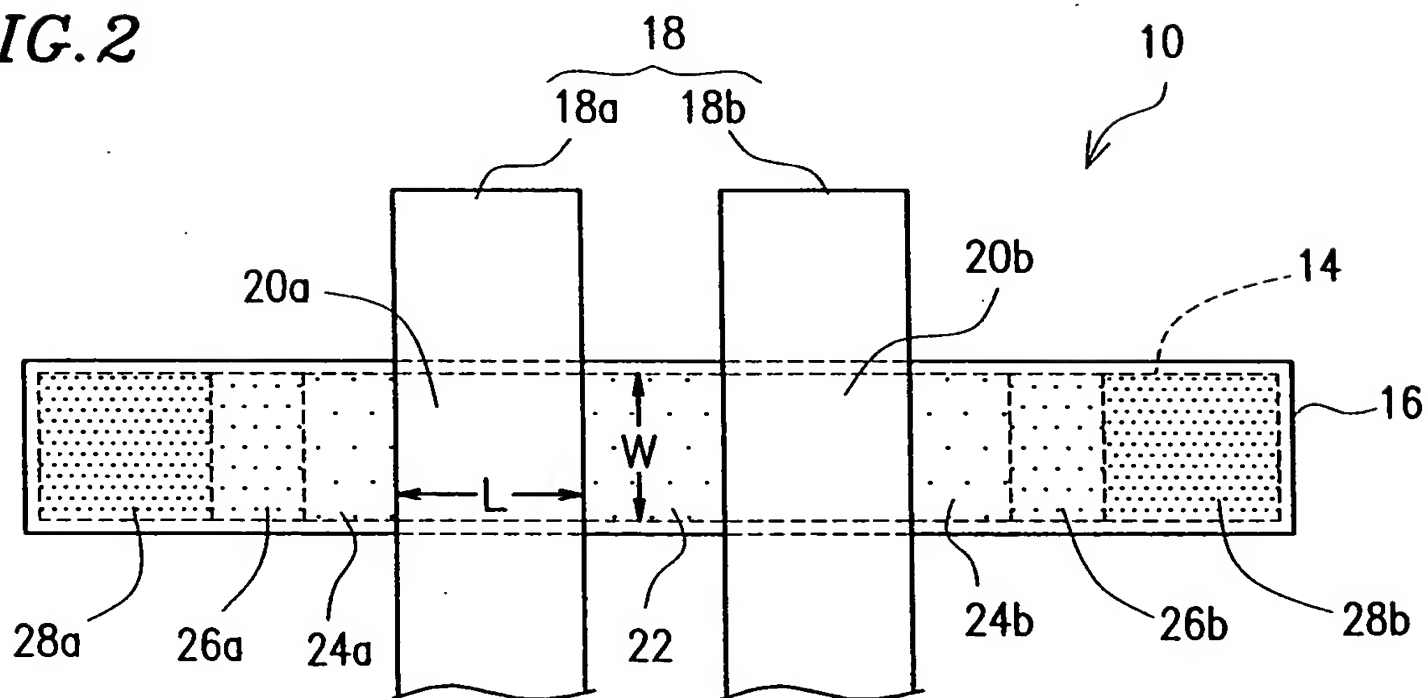




FIG. 3

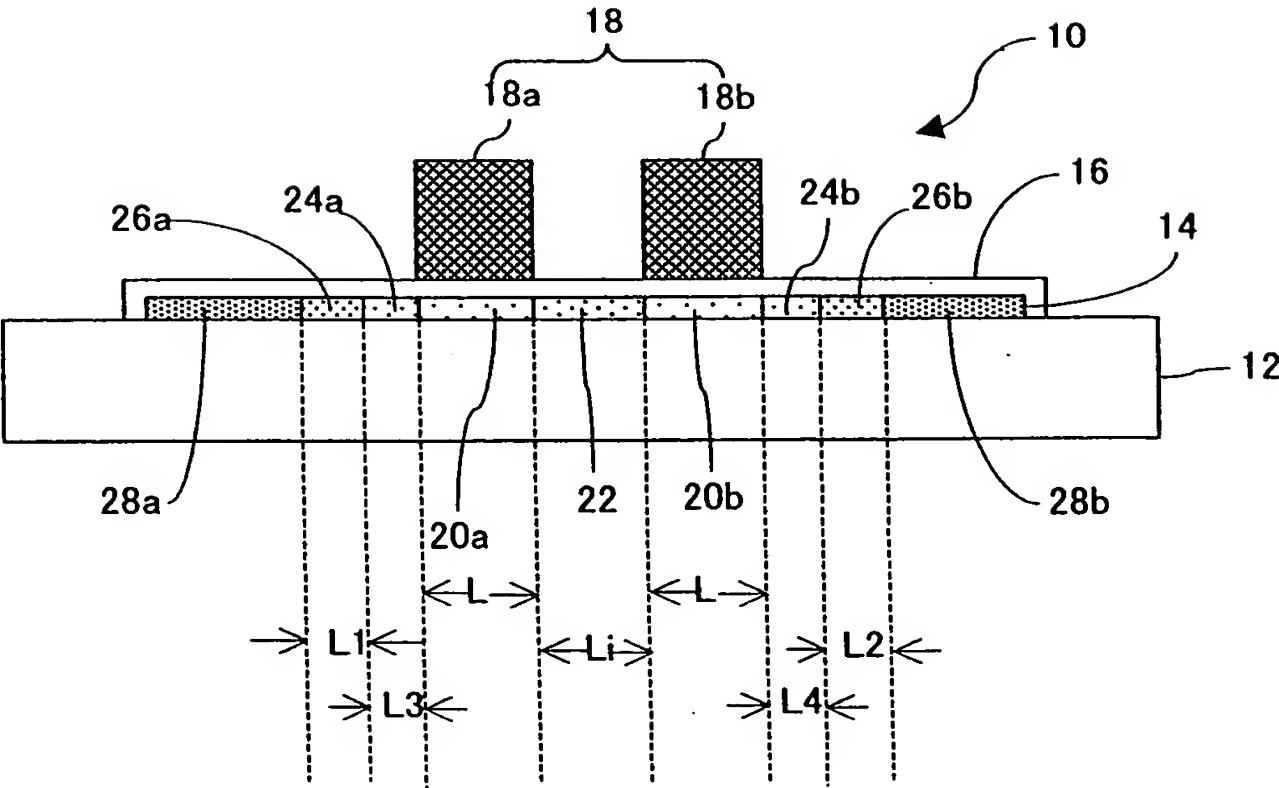




FIG. 4A

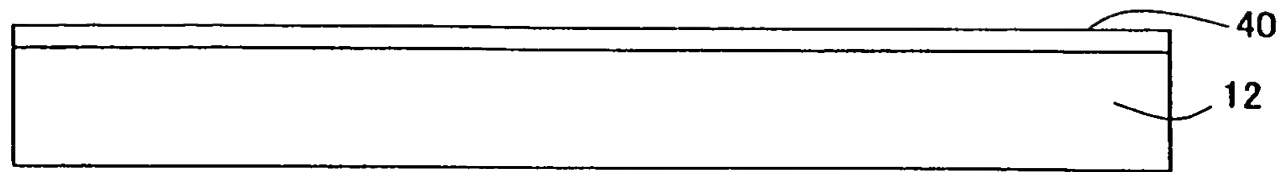


FIG. 4B

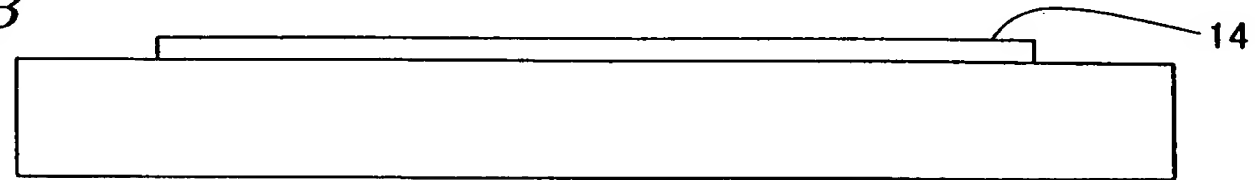


FIG. 4C

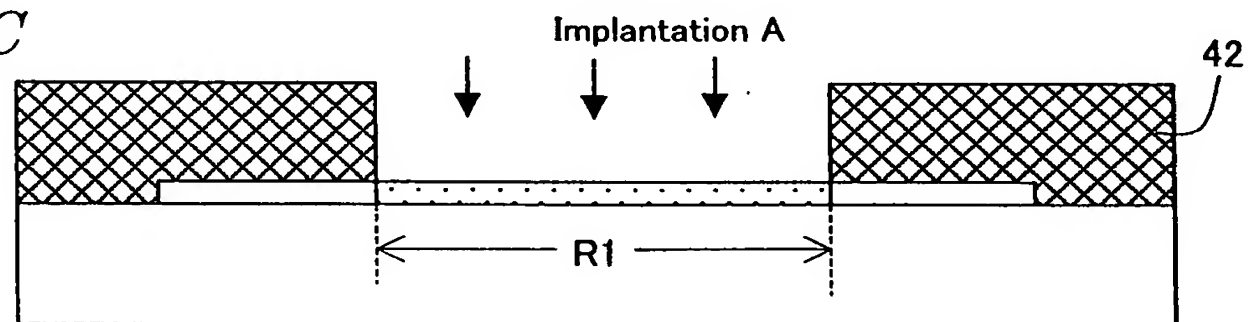


FIG. 4D

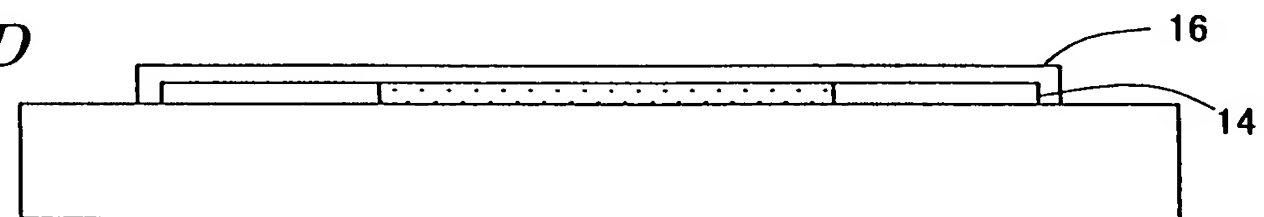


FIG. 4E

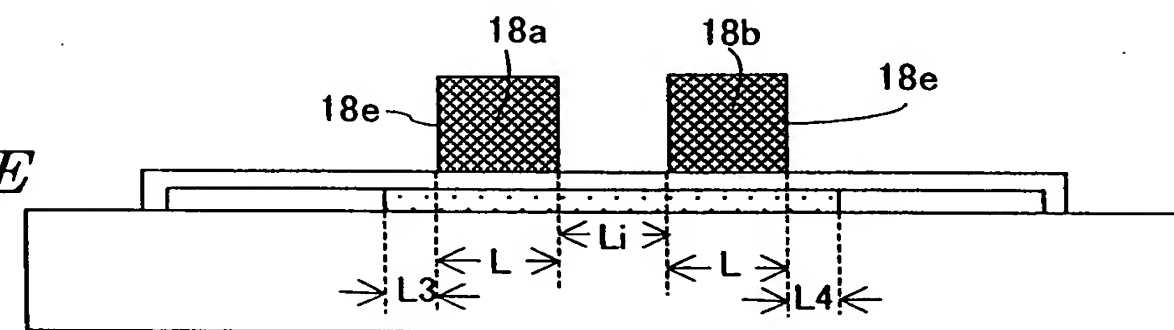
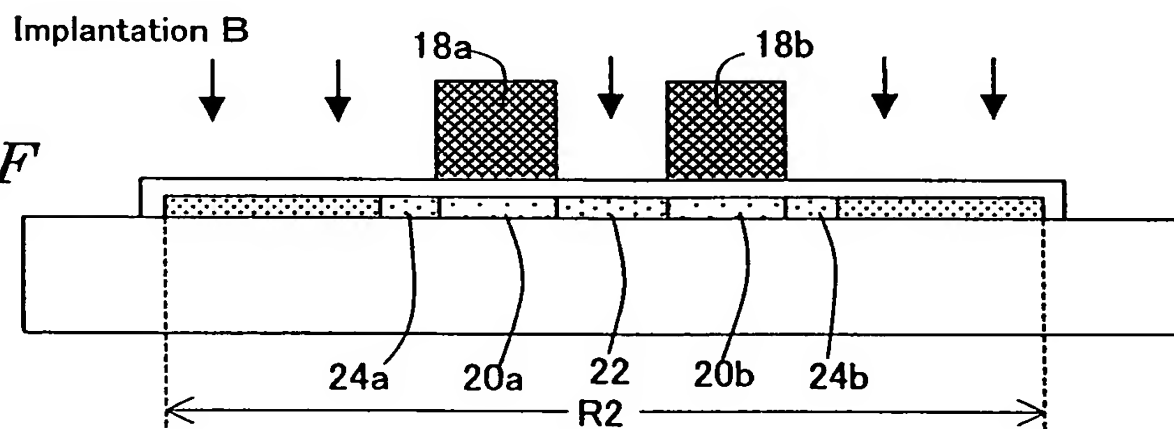


FIG. 4F



[illegible]

This cross-sectional view shows a semiconductor device with a trench isolation structure. A substrate 28a is at the base, with a layer 28b on top. A trench 46 is formed in the substrate, with a bottom layer 48. A trench isolation structure 50 is formed in the trench, with a top layer 52 and a bottom layer 54. The trench isolation structure 50 is formed by a trench 46, a bottom layer 48, and a trench isolation structure 50.

Fig. 1 is a cross-sectional view of a semiconductor device. It shows a substrate 54 with a base layer 56 and a top layer 59. A central region 57 is defined by two vertical structures 58.



FIG. 5A

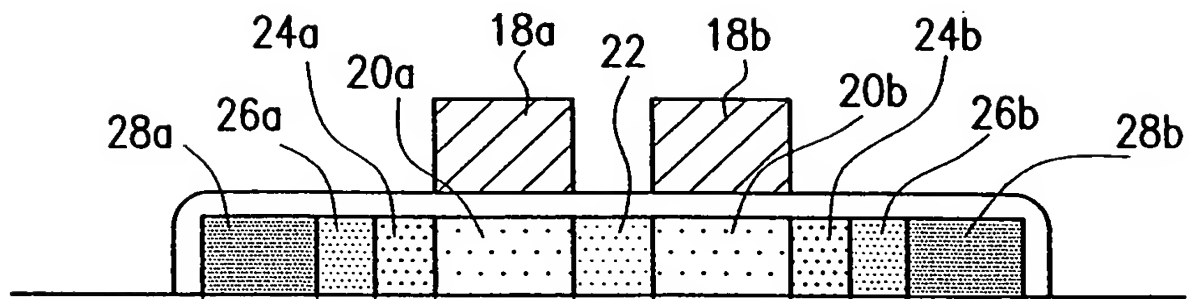


FIG. 5B

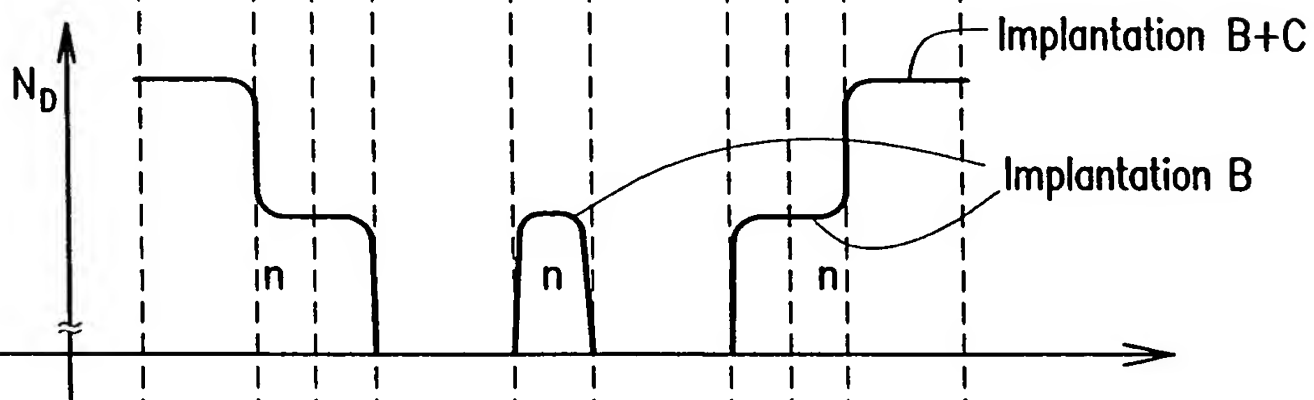


FIG. 5C

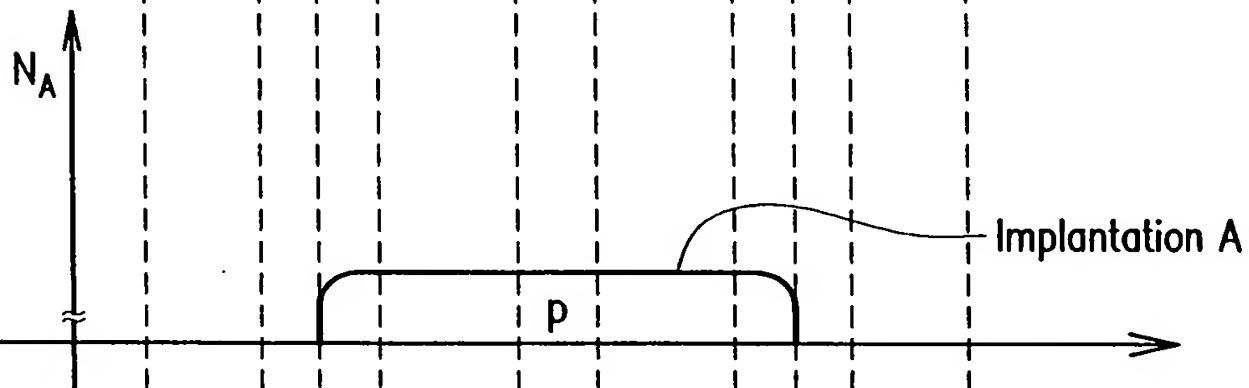


FIG. 5D

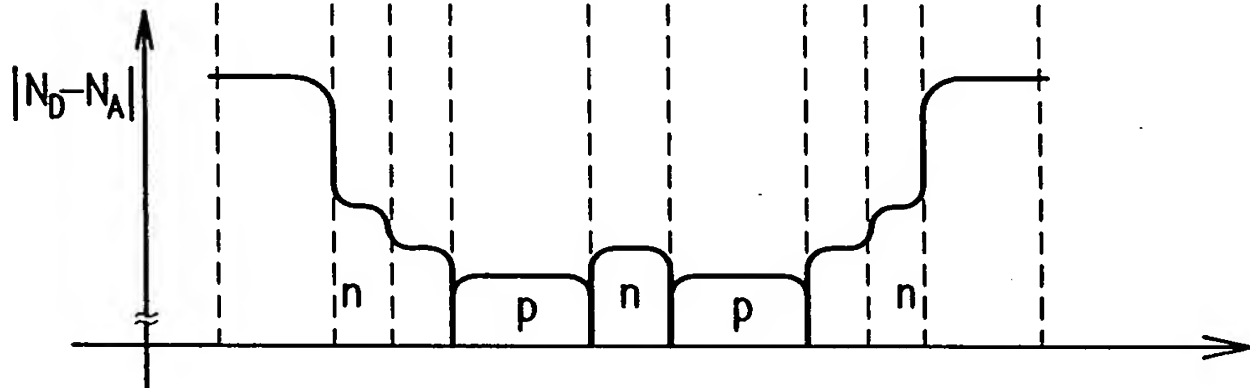




FIG. 6

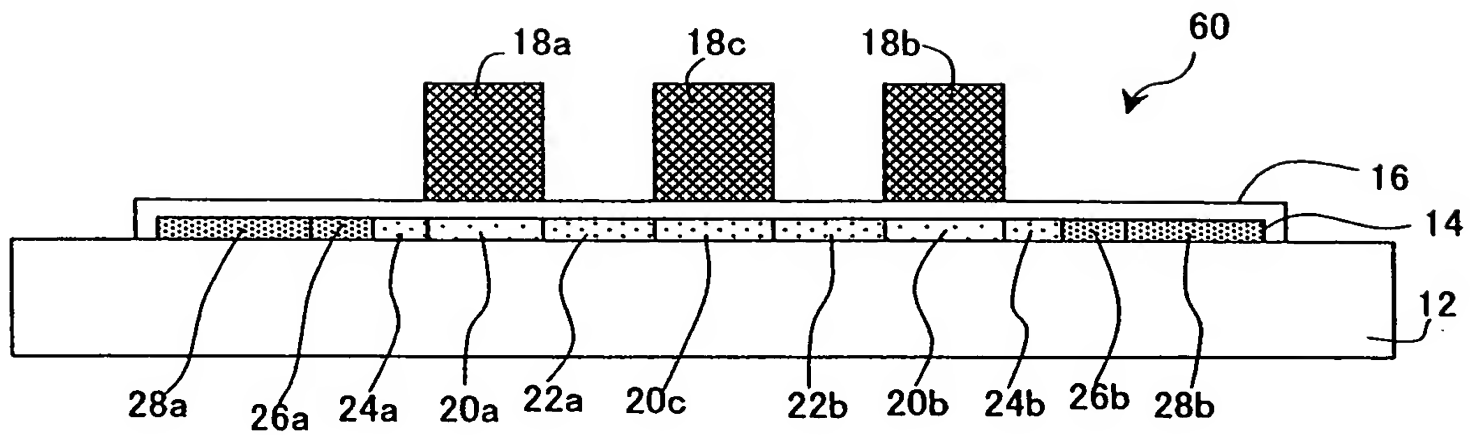


FIG. 7

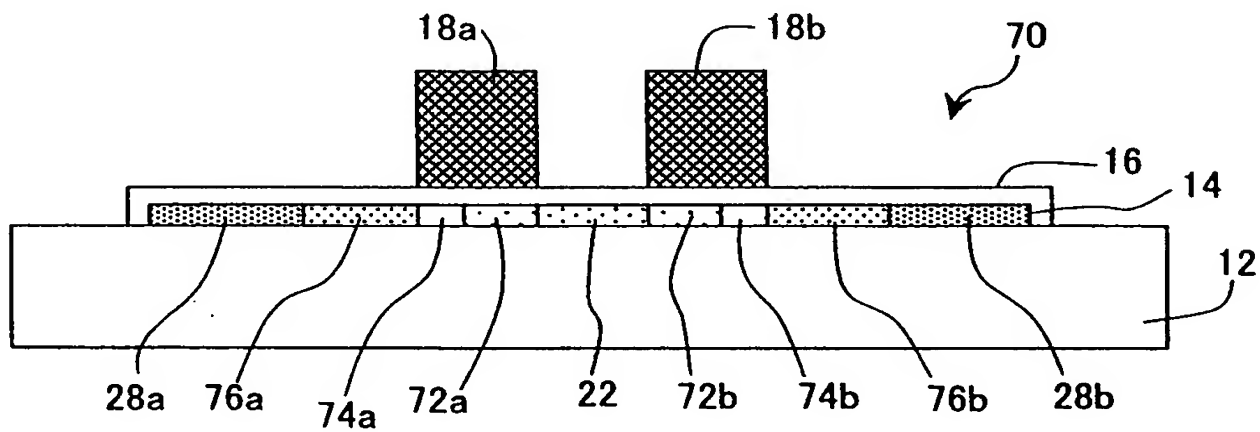




FIG. 8A

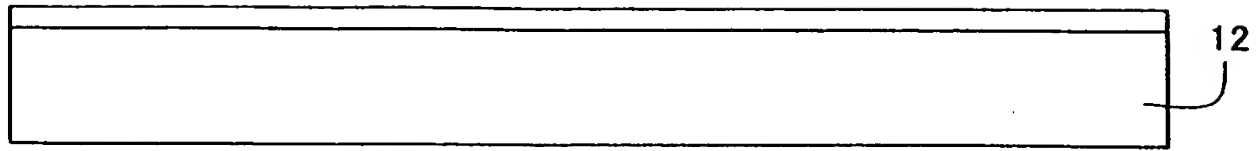


FIG. 8B

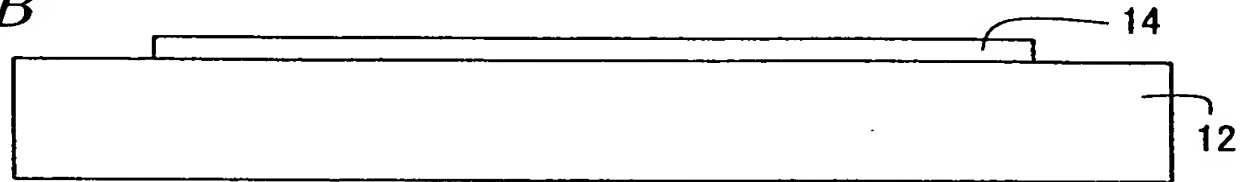


FIG. 8C

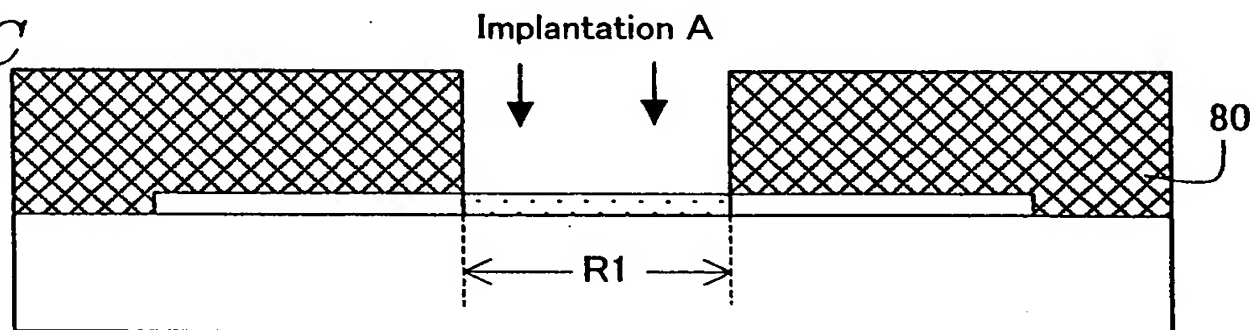


FIG. 8D

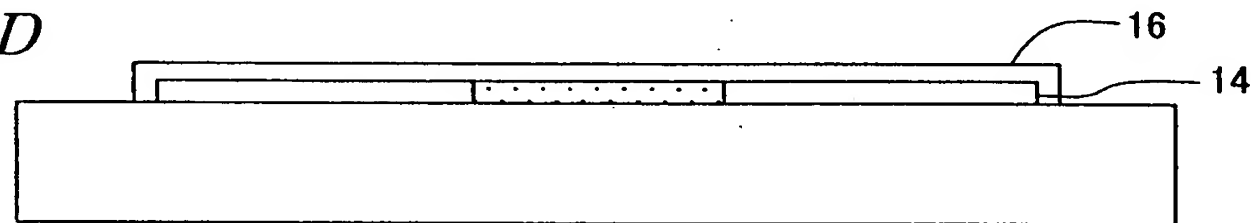


FIG. 8E

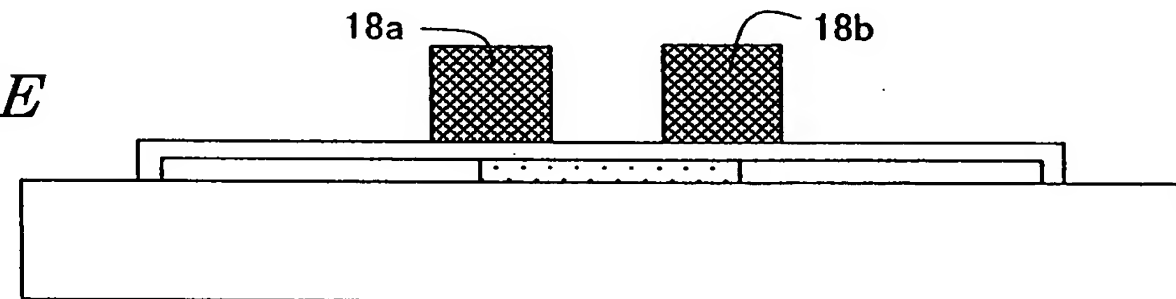


FIG. 8F

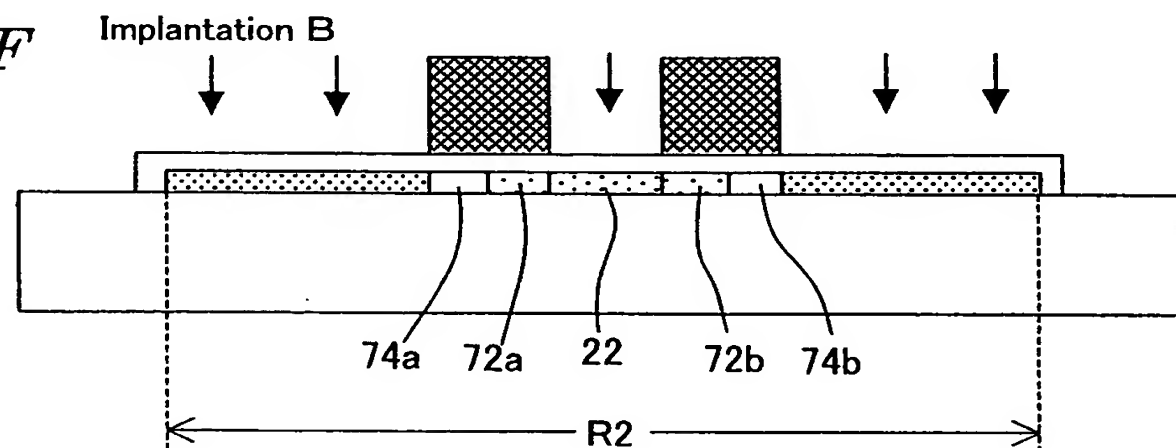




FIG. 8G

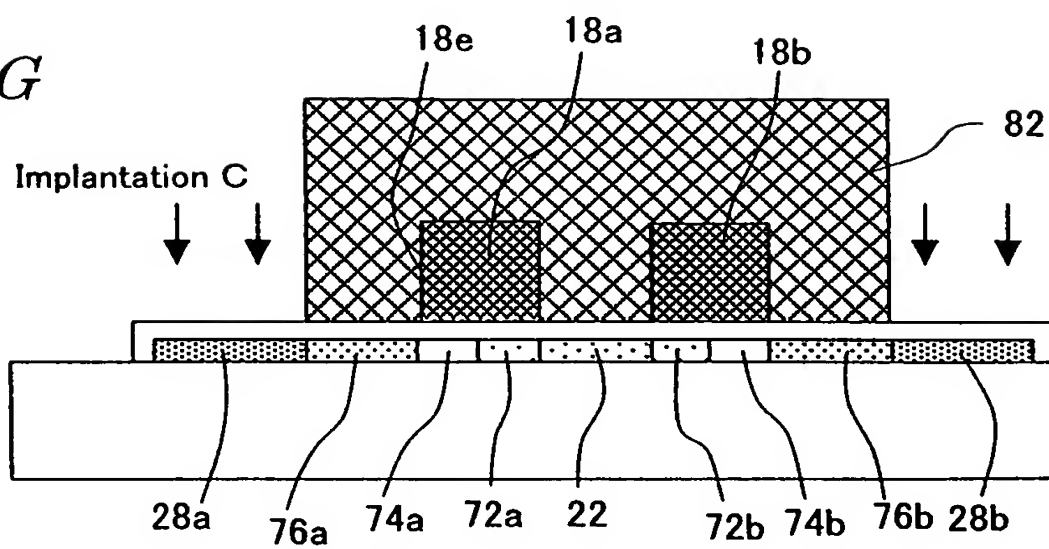


FIG. 8H

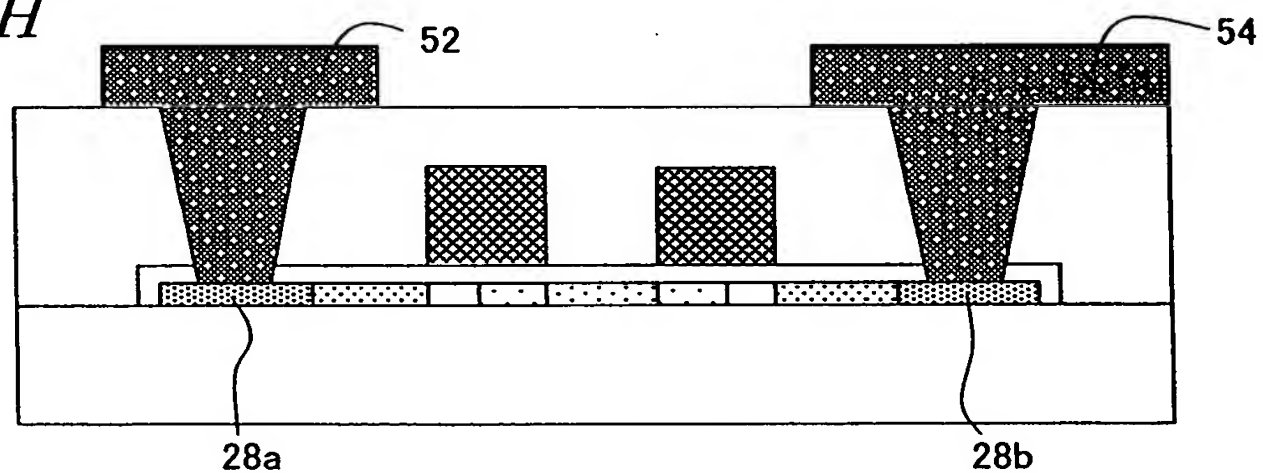


FIG. 8I

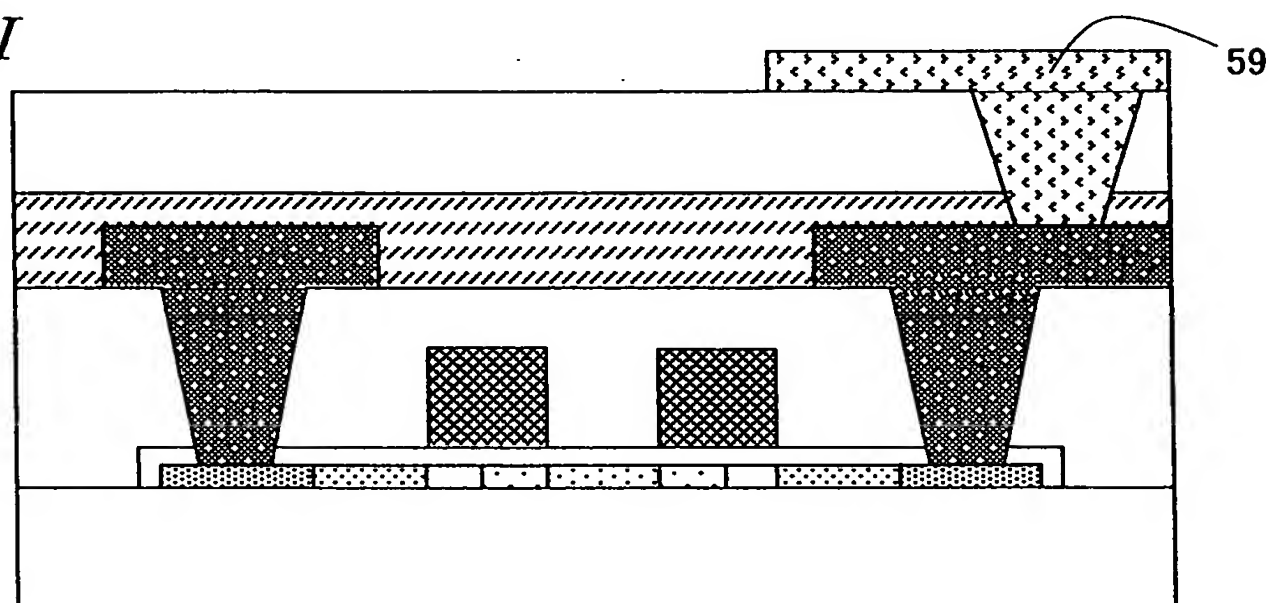




FIG. 9A

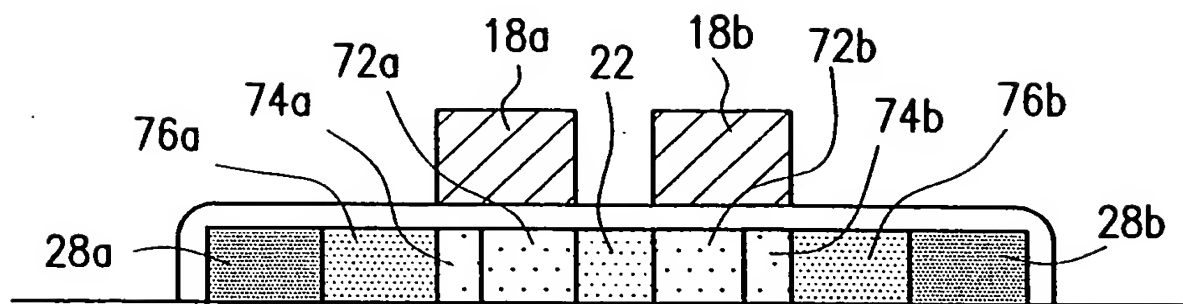


FIG. 9B

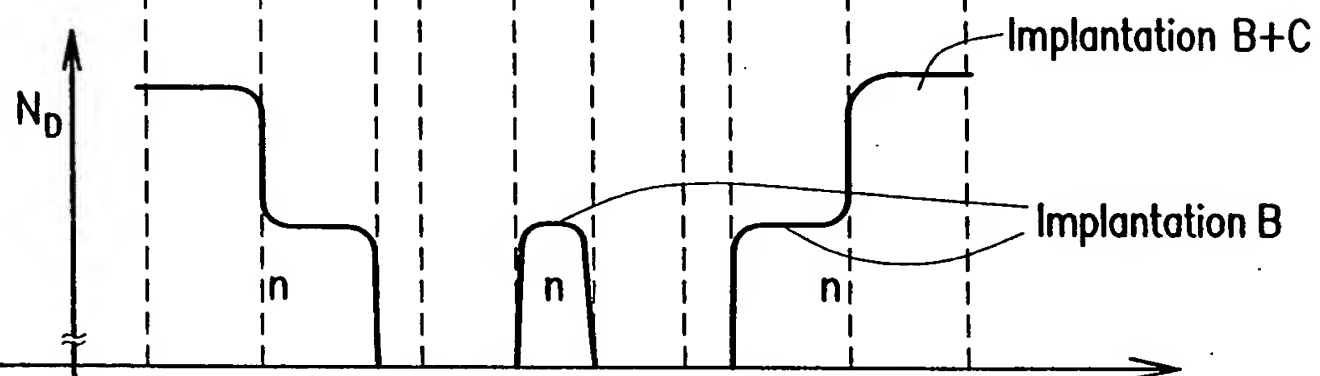


FIG. 9C

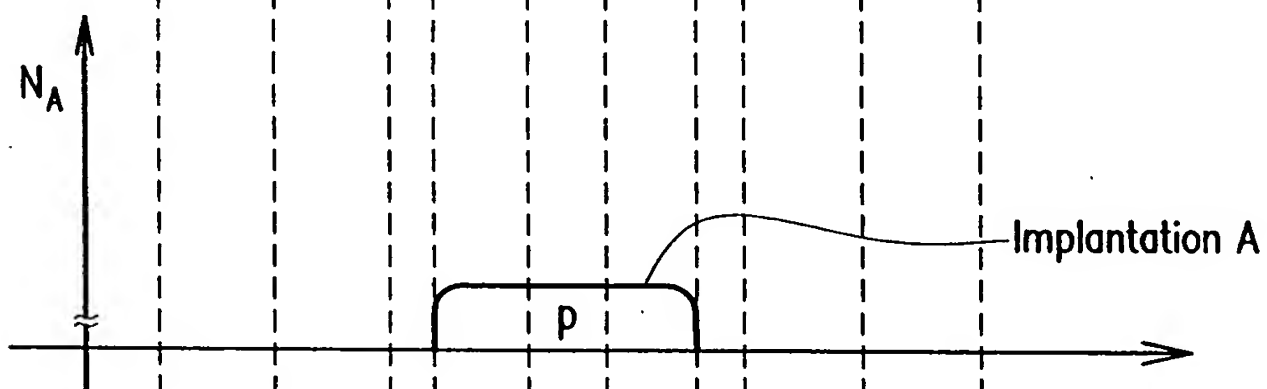


FIG. 9D

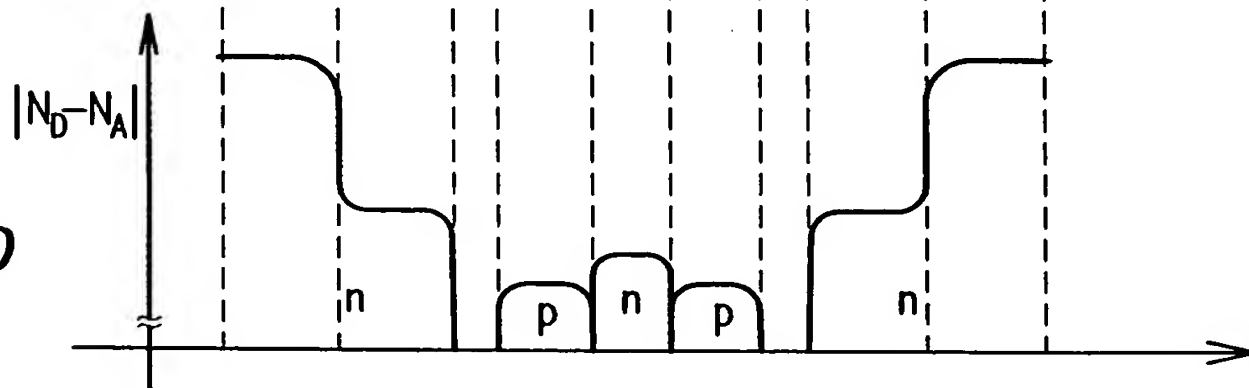




FIG. 10

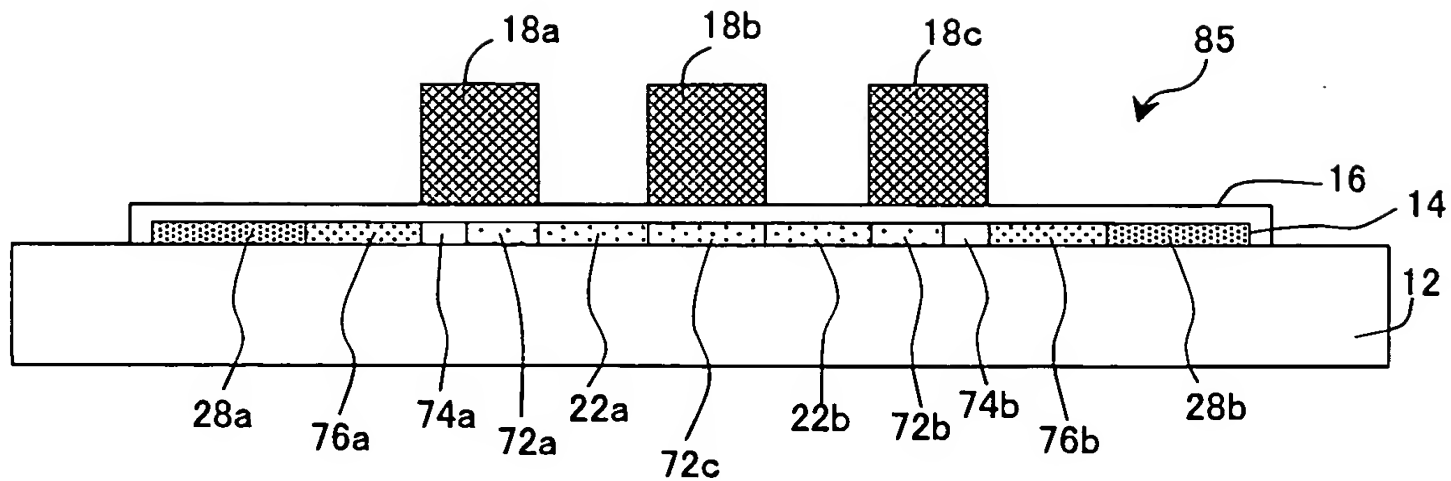


FIG. 11
Prior Art

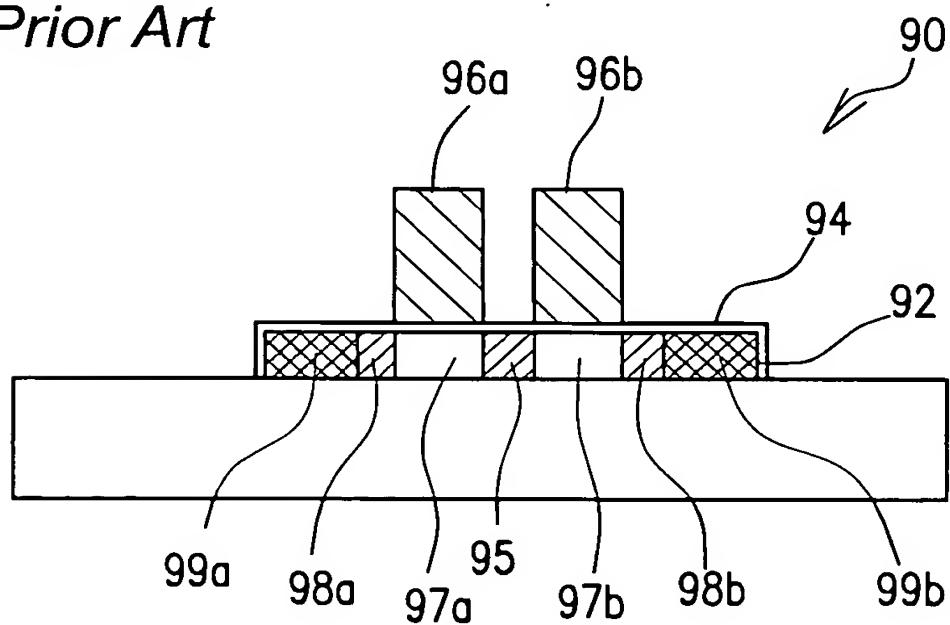




FIG. 12A
Prior Art

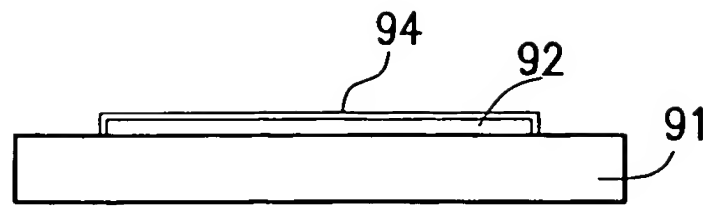


FIG. 12B
Prior Art

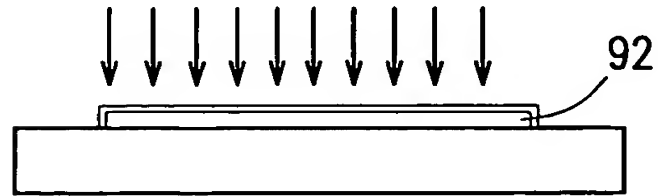


FIG. 12C
Prior Art

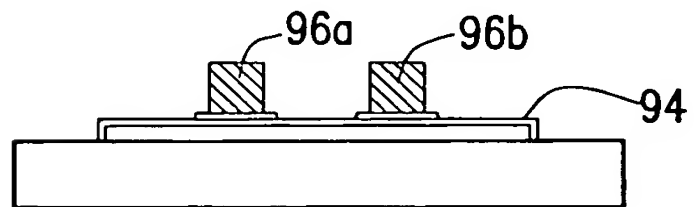


FIG. 12D
Prior Art

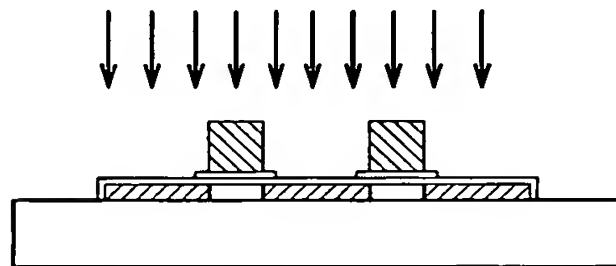


FIG. 12E
Prior Art

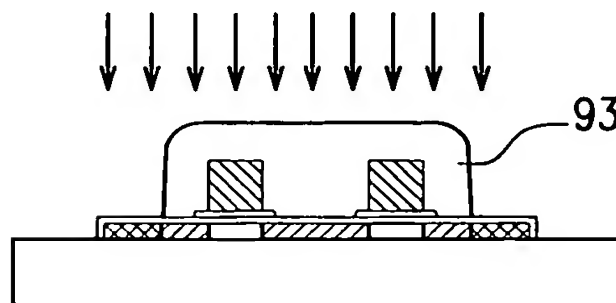


FIG. 12F
Prior Art

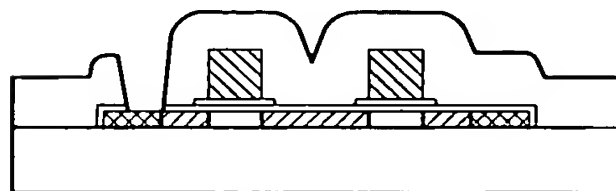


FIG. 12G
Prior Art

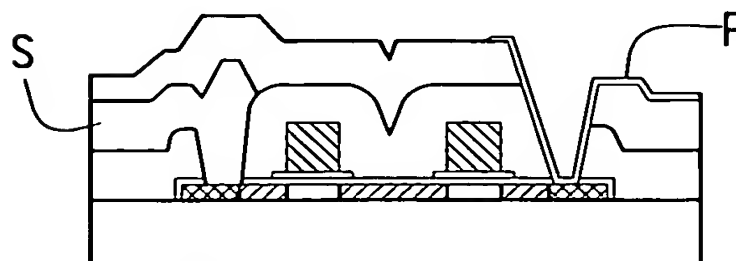




FIG. 13

